REMARKS/ARGUMENTS

The Applicants gratefully acknowledge the Examiner's indication of allowably subject matter in claims 16-17. Reconsideration of the rejected claims is hereby requested. The Specification has been amended to correct several typographical errors.

Recitation of the Invention as-claimed:

In one aspect of the invention, as recited in claim 1, there is provided a method of making a charge-coupled device. In the method, an electrically conducting charge transfer channel is formed in a semiconductor substrate. An electrically insulating layer is formed on a surface of the substrate, and a layer of gate electrode material is formed on the insulating layer.

In accordance with the invention there is formed on the gate material layer a first patterned masking layer having apertures that expose regions of the underlying gate material layer that are to form gate electrodes. The first-pattern-exposed regions of the gate material layer are electrically doped. Further in accordance with the invention a second patterned masking layer is formed on the gate material layer, the second masking layer having apertures that expose regions of the underlying gate material layer that are to form gaps between gate electrodes. The second-pattern-exposed regions of the gate material layer are etched.

The first-pattern-exposed regions of the gate material layer can be electrically doped before the second-pattern-exposed regions of the gate material layer are etched, as recited in claim 4, but such is not in general required, and is not required by the invention as recited in claim 1.

Rejections of the Claims:

Claims 1-10, 12, 14-15, and 18-20 were rejected under 35 U.S.C. §102(b) as being anticipated by Rhodes, U.S. No. 4,742,016. The Applicants concur that Rhodes teaches forming an electrically conducting charge transfer channel in a semiconductor substrate, and forming an electrically insulating layer on a surface of the substrate.

Tuning to formation of gate electrodes, Rhodes explains that he etches and dopes gate electrodes 24 in the "conventional fashion," (Col. 4, lines 3-14). Rhodes forms a "uniform layer of polysilicon suitably doped" and then "pattern[s] the layer appropriately." No specific gate electrode doping or etching processes are taught or even suggested by Rhodes; doping in the "conventional fashion" and "appropriate" patterning are instead suggested. Following convention then, Rhodes specifies forming a "uniform layer," i.e., blanket layer, of polysilicon, the full extent of which is doped in the conventional manner. In other words, if one is to follow Rhodes "conventional" process, a blanket polysilicon layer is blanket-doped before etching the layer to form the gate electrodes 24.

Thus, Rhodes does not employ a mask to form gate electrodes from a "uniform layer of polysilicon suitably doped." This is in direct contrast to the requirements of the claims, which require that only regions of a gate material layer that are exposed by apertures in a patterned masking layer be electrically doped.

The Examiner points to Rhodes Fig. 4 as teaching the formation of a first patterned masking layer having apertures that expose regions of the underlying gate material layer that are to form gate electrodes, and points to Rhodes Col. 4, lines 20-35 as teaching electrically doping the first-pattern-exposed regions of the gate material layer.

In Rhodes Fig. 4 and Col. 4, lines 20-35, there is taught a masking layer 26 used to selectively dope the substrate, not the gate electrodes 24. Rhodes gate electrodes are at this point already formed and doped, as prescribed by Rhodes at Col. 4, lines 3-14, previous to the substrate doping description. Beginning at Col. 4, line 19, Rhodes explains that the "storage region" of the substrate is defined by this ion implantation doping step and the resulting substrate doping is indicated by ++++ signs and reference numeral 31 in the substrate in Fig. 4.

Rhodes does not teach or suggest doping of the gate electrodes with this substrate doping step, which is carried out with ion implantation. Based on the ion implantation dose and energy specified by Rhodes (1.2×10^{12} ions at 200 KeV) one can only know that the substrate is doped, and can imply nothing more. Given the thickness of Rhodes' previously formed and doped gate electrodes, one cannot imply that the gate electrodes are doped by this step. Certainly this is not the intention of Rhodes because the gate electrode had been previously blanket-doped and etched in the conventional fashion, as described above and given at Rhodes Col. 4, lines 3-14, before undertaking this substrate storage region doping step.

The Applicants therefore respectfully submit that the Examiner mistook Rhodes substrate storage region doping for gate electrode doping. As explained above, Rhodes uses "conventional" doping, including blanket-doping of a "uniform layer of polysilicon suitably doped," and "appropriate" patterning processes, prior to the substrate storage region doping step. The blanket-doping by Rhodes of a polysilicon gate layer is in direct contradiction to the doping of pattern-exposed regions required by claim 1.

The Examiner points to Rhodes Col. 4, lines 40-57 as teaching the formation of a second patterned masking layer having regions exposing the underlying gate material. The Applicants respectfully submit that the Examiner is mistaken. In the Rhodes passage cited by the Examiner, beginning at Col. 4,

line 36, Rhodes explains that a gate oxide layer 22 is "etched back," that is, completely removed, from the storage regions 31 of the substrate that were just doped in the previous step just described above. This etch-back step aligns the edges of the gate electrode 34 with the underlying oxide 22. Rhodes Col. 4, lines 36-42 describe this removal of the gate oxide layer.

At lines 43-57 of the cited passage Rhodes describes the growth of a "second oxide layer," (line 49). No patterned masking layer at all is taught or even hinted at in the Col. 4, lines 40-57 passage cited by the Examiner, let alone a masking layer exposing regions of an underlying gate layer.

The Examiner referred to Rhodes Fig. 6 as teaching etching second-pattern-exposed regions of a gate material layer. In Rhodes Fig. 6 is shown a "second phase set of gate electrodes" 28 (Col. 4, lines 58-59). Rhodes prescribes the formation of this second set of gate electrodes in precisely the manner given for formation of the first gate electrodes: "a layer of suitably doped polysilicon...is deposited...and then patterned in conventional fashion to arrive at the structure shown in Fig. 6," (Col. 4, lines 60-63). In other words, the second gate electrodes are formed by blanket-doping and then patterned etching, just as were Rhodes first electrodes 24. This is in direct contradiction to the patterned doping required by the claims.

Further, it is important to note that claim 1 requires performance of all steps on one and the same gate material layer: Claim 1 requires forming a first patterned masking layer on a gate material layer, doping first-pattern-exposed regions of <u>the</u> gate material layer, forming a second patterned masking layer on <u>the</u> gate material layer, and etching second-pattern-exposed regions of <u>the</u> gate material layer. All masking, doping, and etching steps are performed on one common, single gate material layer.

But the Examiner has construed Rhodes processing of two distinct and separated gate layers as the single gate layer processing of claim 1. Rhodes fails to teach or even suggest the first masking layer formation, doping, second masking layer formation, and etching of a single layer required by the claims.

Claims 2-10, 12, and 14-15 all depend from claim 1 and all require the limitations of claim 1 discussed above and missing from Rhodes. Similarly, independent claims 18-20 require the limitations of claim 1 discussed above and missing from Rhodes. The Applicants therefore submit that Rhodes neither teaches nor suggests the methods of claims 1-10, 12, 14-15, and 18-20.

Claim 2 further requires that the first patterned masking layer be removed after electrically doping first-pattern-exposed regions of the gate material layer. The Examiner here refers to Rhodes Col. 4 lines 20-35 discussed above, suggesting that Rhodes teaches such. As explained above, the doping step of this Rhodes passage is directed to the substrate, not the gate electrodes. Rhodes had already blanket-doped the gate electrode layer prior to the substrate doping step, and one cannot expect that the substrate doping further dopes the gate electrodes. Rhodes removal of a masking layer described at this passage is carried out after doping of the substrate, not the gate electrodes. No masking layer is employed by Rhodes to dope the gate electrode layer.

Claim 3 further requires that the second patterned masking layer be removed after etching second-pattern-exposed regions of the gate material layer. The Examiner here refers Rhodes Col. 4, lines 40-57, as teaching such. As explained above, this passage describes an oxide etch-back step to align the edges of the gate electrode 34 with the underlying oxide 22. Rhodes Col. 4, lines 36-42 describe this removal of the gate oxide layer. At lines 43-57 of the cited passage Rhodes describes the growth of a "second oxide layer," (line 51). No patterned masking layer at all is taught or even hinted at in the Col. 4, lines 40-57 passage

cited by the Examiner, let alone a masking layer exposing regions of an underlying gate layer. No removal of a masking layer can therefore occur.

Claim 4 further requires that the first-pattern-exposed regions of gate material be electrically doped before second-pattern-exposed regions of gate material are etched. The Examiner here refers to Rhodes Col. 4 lines 20-35 discussed above, suggesting that Rhodes teaches such. As explained above, at this cited Rhodes passage, the gate electrodes have already been etched. Masking is carried out as part of a substrate doping process. Thus, even if the Examiner is to suggest that cited substrate doping process dopes the gates, the gates have already been etched at this doping step. The Rhodes sequence of first etching then doping would be exactly the opposite of that required by claim 4. But more broadly, Rhodes does not teach the patterned gate material doping step required by claim 4 as well as all other claims.

Claim 5 further requires ion implantation of a selected dopant into first-pattern-exposed regions of a gate material layer. The Examiner here refers to Rhodes Col. 4 lines 20-35 discussed above, suggesting that Rhodes teaches such. As explained, this passage refers to substrate doping, not gate electrode layer doping.

Claim 6 further requires that the etching of second-pattern-exposed regions of a gate material layer be plasma etching. The Examiner here refers Rhodes Col. 4, lines 40-57, as teaching such. This passage does not once even mention "plasma etching," and Rhodes does not teach or even suggest such. As explained above, this passage describes an oxide etch-back step to align the edges of the gate electrode 34 with the underlying oxide 22. Rhodes Col. 4, lines 36-42 describe this removal of the gate oxide layer, but no specific etch technique is given at all. At lines 43-57 of the cited passage Rhodes describes the growth of a "second oxide layer," (line 51). No patterned masking layer at all is taught or

even hinted at in the Col. 4, lines 40-57 passage cited by the Examiner, let alone a masking layer exposing regions of an underlying gate layer.

Claim 7 further requires heat treating the electrically-doped and etched gate electrode material to diffuse electrical dopant through the gate material layer thickness. Claim 8 requires that the heat treating be annealing. The Examiner here refers to Rhodes Col. 5, lines 4-27 as teaching such. At this Rhodes passage there is described "a high temperature step used to diffuse the arsenic implanted in the first oxide layer out into the underlying silicon," (Col. 5, lines 4-6). This step is directed to the doping of the substrate by diffusing dopant from an oxide layer atop the substrate into the substrate itself. No teaching or even suggestion of using this step to for diffusing dopant through the gate material is given. Instead, Rhodes requires that the heat treating be a tailored annealing step to "minimize problems arising from variation of channel potentials in the storage region of the first-phase set of electrodes," (Col. 5, lines 8-10). The storage region of the substrate, described above, is defined by an ion implantation doping step and the resulting storage region is indicated by ++++ signs and reference numeral 31 in the substrate in Fig. 4. The annealing referred to in Col. 5 results in a doped substrate regions indicated by ++++ signs and reference numeral 30 in the substrate in Fig. 6. Nothing more can be implied from this process as Rhodes explicitly requires it to be tailored for defining the substrate doping.

Claim 9 further requires that the heat treating be oxidation of the gate material layer. The heat treating technique of Rhodes described at Rhodes Col. 5 does not teach or even suggest oxidizing gate material. It is solely directed to diffusing dopant out of an oxide layer 21 into the underlying substrate 20 as shown in Fig. 6. The description is simply devoid of a suggestion for a gate oxidation technique.

Claim 10 further requires that first and second masking layers each have a pattern of apertures that are characterized by an extent which accounts for lateral dopant diffusion during heat treatment. This is shown in Fig. 4D of the instant application and described at Page 14, lines 20+ of the instant application. In Fig. 4D there is shown a gate material layer 18 which has been selectively doped to form doped regions 42, the edges of which are indicated with dotted lines. A second patterned masking layer of photoresist 40 is shown atop of the gate layer. As explained in the instant application, the photoresist regions 44 that shield the doped rage layer regions 42 preferably extend beyond the edges of the doped gate layer regions to account for subsequent lateral dopant diffusion.

The Examiner refers to Col. 4, lines 20-57 and Col. 5, lines 4-27 to Rhodes as teaching such. The Applicants submit that nowhere in Rhodes is there shown or even suggested an arrangement of mask aperture extent that accounts for lateral dopant diffusion as required by claim 10. Rhodes blanket dopes a gate material layer and etches such in the conventional fashion. As a result, Rhodes has absolutely no concern with lateral diffusion through a gate material layer. Even if the oxide-to-substrate dopant diffusion step at Rhodes Col. 5 were to be considered a gate electrode annealing step, at that point the gate electrode is already etched and therefore it would be nonsensical for Rhodes to consider lateral gate electrode diffusion at that step.

Claim 12 requires that the electrically insulating layer formed on the substrate surface be a layer of oxide. As discussed previously, the Applicants concur that Rhodes forms a layer of oxide on the substrate surface. But for any oxide layer formation, Rhodes fails to teach or even suggest the gate electrode layer doping and etching steps required by all of the claims, as explained above.

Claim 14 further requires that forming a gate electrode layer be carried out by depositing a layer of polysilicon on an insulating layer. The Applicants concur that Rhodes forms suggest forming a layer of polysilicon in the

conventional manner. But for any polysilicon layer formation, Rhodes fails to teach or even suggest the gate electrode layer doping and etching steps required by all of the claims.

Claim 15 requires that the first and second masking layers each be photoresist that is photolithographically patterned. The Examiner here refers to Rhodes Col. 4, lines 20-57 as teaching such. As explained above, this Rhodes passage refers to a doping step for doping the substrate, not the gate electrodes. Rhodes suggests that a mask that is patterned is here employed, but no specific patterning process is taught or suggested by Rhodes. Even if photolithography is employed by Rhodes, for mask formation, Rhodes fails to teach or even suggest the gate electrode layer doping and etching steps required by all of the claims.

Claims 11 and 13 were rejected under 35 U.S.C. §103(a) as being unpatentable over Rhodes in view of Erhardt, U.S. No. 5,114,833.

Claim 11 requires that the forming of an electrically conducting charge transfer channel in a semiconductor substrate comprise ion implantation of a selected electrical dopant into the substrate.

In Rhodes Fig. 4 and Col. 4, lines 20-35, there is taught a masking layer 26 used to selectively dope the substrate, as explained in detail above. Beginning at Col. 4, line 19, Rhodes explains that the "storage region" of the substrate is defined by this ion implantation doping step and the resulting substrate doping is indicated by ++++ signs and reference numeral 31 in the substrate in Fig. 4. Therefore Rhodes does teach the use of ion implantation into a substrate. But as explained above, this ion implantation step is indeed directed to forming a charge transfer channel in the substrate and is not directed to doping of a gate electrode layer. For any charge transfer channel formation technique, Rhodes fails to teach or suggest the suggest the gate electrode layer doping and etching steps required by all of the claims.

Claim 13 requires that the gate electrode material be deposited as a layer of amorphous silicon. The Examiner refers to Erhardt here, but the Examiner does not actually cite any figure or passage in Erhardt that teaches the use of amorphous silicon. Neither Erhardt nor Rhodes teach or suggest the use of amorphous silicon. Both Erhardt and Rhodes employ polysilicon: Erhardt at Col. 2, lines 40-41 specifies "polysilicon gate electrodes 20 and 22." Rhodes uses "gate electrodes 24, advantageously of polysilicon, as is usual in such devices," (Col. 4, lines 5-6). Neither Erhardt nor Rhodes, nor any combination of the two, teach or suggest the use of amorphous silicon as a gate electrode material.

The Applicants therefore submit that the claims are in condition for allowance, which action is requested.

If the Examiner has any questions or would like to discuss the claims, he is encouraged to telephone the undersigned Agent directly at his convenience at the phone number given below.

An Information Disclosure Statement accompanies this response.

Respectfully submitted,

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